WHAT IS CLAIMED IS:

1. A power control device for controlling an amount of power to be consumed in a processor, the power control device comprising:

a power table including a plurality of power control registers each rewritably storing power control information;

a condition determiner for rewritably storing a plurality of operating conditions and determining which one of the plurality of operating conditions is satisfied by a current operation of the processor so as to supply an index signal to select one of the plurality of power control registers based on the determination; and

a controller for controlling a power consumption in the processor according to the power control information in one of the power control registers that is selected by the index signal.

2. The power control device of claim 1, wherein the power control information includes block information for specifying one or more circuit block to be subjected to a power control by the controller.

3. The power control device of claim 1, wherein the power control information includes voltage information representing a magnitude of a power supply voltage to be supplied to a control object circuit block.

4. The power control device of claim 1, wherein the power control information includes voltage information for

controlling a threshold voltage of each transistor of a control object circuit block.

5. The power control device of claim 1, wherein the power control information includes clock information representing a frequency of a clock to be supplied to a control object circuit block.

6. The power control device of claim 1, wherein the power control information includes clock information representing whether or not to terminate a supply of a clock to a control object circuit block.

7. The power control device of claim 1, wherein the condition determiner includes:

an address table including a plurality of register means each rewritably storing a comparison address and an index number associated with the comparison address;

means for determining which one of the plurality of comparison addresses matches an address indicated by a program counter of the processor; and

means for supplying, to the power table as the index signal, a signal representing an index number associated with the comparison address that has been determined to be a match.

8. The power control device of claim 7, wherein the condition determiner further includes means for performing a control so that the match determination is performed only when a discontinuous change is detected in the address indicated by the program counter.

9. The power control device of claim 1, wherein the condition determiner includes:

an address table including a plurality of register means each rewritably storing a comparison start address, a comparison end address associated with the comparison start address, and an index number associated with the comparison start address and the comparison end address;

means for determining one of a plurality of address ranges each defined by one of the comparison start addresses and one of the comparison end addresses to which an address indicated by a program counter of the processor belongs to; and

means for supplying, to the power table as the index signal, a signal representing an index number associated with the comparison start address and the comparison end address defining the address range that has been determined to include the indicated address.

10. The power control device of claim 1, wherein the condition determiner includes:

an event table including a plurality of register means each rewritably storing a comparison event type and an index number associated with the comparison event type;

means for determining which one of the plurality of comparison event types matches a type of an event that has occurred in the processor; and

means for supplying, to the power table as the index

signal, a signal representing an index number associated with the comparison event type that has been determined to be a match.

11. The power control device of claim 1, wherein the condition determiner includes:

a time table including a plurality of register means each rewritably storing a comparison time and an index number associated with the comparison time;

means for determining which one of the plurality of comparison times matches a time indicated by a time signal from the processor; and

means for supplying, to the power table as the index signal, a signal representing an index number associated with the comparison time that has been determined to be a match.

12. The power control device of claim 1, wherein the condition determiner includes:

a time table including a plurality of register means each rewritably storing a comparison start time, a comparison end time associated with the comparison start time, and an index number associated with the comparison start time and the comparison end time;

means for determining one of a plurality of time periods each defined by one of the comparison start times and one of the comparison end times to which a time indicated by a time signal from the processor belongs to; and

means for supplying, to the power table as the index

signal, a signal representing an index number associated with the comparison start time and the comparison end time defining the time period that has been determined to include the indicated time.